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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/862,941
Filing Date: May 22, 2001
Appellant(s): FLOOD ET AL.

Himanshu Amin
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 5/27/08 appealing from the Office action mailed 12/27/07.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is not correct. Appealed claims are 1, 3-53, and claim 2 is canceled.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

4,807,259	**Yamanaka et al.**	2-1989
6,199,169	**Voth**	3-2001
6,449,732	**Ramussen et al.**	9-2002
6,775,246	**Kuribayashi et al.**	8-2004

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

DETAILED ACTION

. Claims 1, 3-53 are pending. Claim 3 has been amended. Claim 2 has been canceled. Independent claims are **1, 38, 39 and 52**.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim **1** is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with

the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Applicant has amended claim 1 with the limitation, *" the time synchronization apparatus is configurable to operate as* ***both*** *a synchronization master and a synchronization slave "*. There is *no disclosure within the specification or original claims* for this limitation. There is disclosure for an apparatus to act as **either** a master **or** a slave. But, there is no disclosure for an apparatus to act as **both** a master and a slave **at the same time** as the claim limitation states.

Appropriate action is required. If applicant feels there is disclosure for this claim limitation, please indicate the required citation for confirmation.

Claim Rejections 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1, 3 - 7, 13 - 28, 30 - 34, 38 - 46, 48 - 53** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yamanaka et al.** (US Patent No. **4,807,259:** Time synchronization method in data transmission system)
) in view of **Voth** (US Patent No. **6,199,169**: System and method for synchronizing time across a computer cluster, Filed Dec. 15, 1998).

Regarding Claim 1, Yamanaka discloses a time synchronization apparatus for synchronizing operation of a first controller with that of a second controller in a control system, the synchronization apparatus comprising:

- a processor interface for interfacing the synchronization apparatus with a host processor, the time synchronization apparatus is configurable to operate as **both** a synchronization master and a synchronization slave; (see Yamanaka Figure 3A; Figure 3B; col. 1, lines 15-22; col. 2, lines 29-37; Figure 3A; col. 5, lines 5-9: configurable to operate as a master; Figure 3B; col. 5, lines 12-18: configurable to operate as a slave)
- a timing system with a clock that maintains an indication of time according to information received from one of the network and the host processor. (see Yamanaka Figure 3A; Figure 3B; col. 4, lines 6-14; col. 6, lines 41-63)

Yamanaka discloses a low bandwidth modem circuit for network connections in the network receipt of synchronization information and data. This type of network

affords limited communications bandwidth and a limited number of possible network configurations and topologies.

However, Voth discloses wherein:

- a transmitter adapted to transmit synchronization information and data to a network in the control system; (see Voth col. 2, lines 57-60)

- a receiver adapted to receive synchronization information and data from the network; (see Voth col. 2, lines 60-61)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability to network communications in a variety of configurations. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30: *" … Based on the preceding discussion, it is not hard to appreciate that a need exists for time synchronization systems that are suitable for use in networks where the ethernet simplification does not apply. … "*; col. 2, lines 39-43: *" … Currently available time synchronization systems may also require the network to process large numbers of synchronization messages. A large number of synchronization messages steal network bandwidth from other computing tasks. … "*)

Regarding Claim 3, Yamanaka discloses the time synchronization apparatus of claim 1, being configured to operate as a synchronization master, the synchronization

apparatus is a hardware module coupled to the host processor. (see Yamanaka Figure 3A; Figure 3B; col. 1, lines 15-22; col. 2, lines 29-37; Figure 3A; col. 5, lines 5-9: configurable to operate as a master; Figure 3B; col. 5, lines 12-18: configurable to operate as a slave) And, Voth discloses wherein the transmitter periodically transmits message frames at a fixed period. (see Voth col. 4, lines 43-47: frames transmitted at a fixed interval)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability to be configured to operate as a synchronization master. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claims 4, 15, Voth discloses the time synchronization apparatus of claim 3, 14, wherein the fixed period is about 50μs. (According to Applicant's specification on page 28 at lines 15-16, it states, *"...the synchronization component can transmit (broadcast) a frame every 50μs or some other fixed time period."* see Voth col. 4, lines 43-54: where the reference states that the update period is performed at a regular or periodic fixed time period which can be equal to 50us or some other time period.)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where a fixed period is about 50μs. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in

order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claims 5, 16, Voth discloses the time synchronization apparatus of claim 3, 14, wherein the transmitter transmits a message frame having an LCM indicator at a least common multiple (LCM) interval. (see Voth col. 4, lines 43-54: *"…use a repeating update cycle…Update cycle…includes an initial calculation … scheduling period…a time adjustment period."* Applicant's specification states on page 13 at lines 20-26 that *"…least common multiple (LCM) period, …can be set to the lowest integer multiple of periodic tasks…"* (i.e. set to 1) Thus, LCM is tied to reference's periodic update cycle.)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability to transmit a message frame having an LCM indicator. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claims 6, 17, Voth discloses the time synchronization apparatus of claim 5, 16, wherein the LCM interval is 600ms. (see Voth col. 4, lines 43-54: *"…use a repeating update cycle…Update cycle…includes an initial calculation…scheduling period…a time adjustment period."* Applicant's specification status on page 13 at lines 20-26 that *"…600ms is exemplary… other LCM periods fall within the scope of the present*

invention…" Thus, LCM is equal to periodic update cycle.)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the LCM interval is 600ms. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claims 7, 30, Voth discloses the time synchronization apparatus of claim 3, 14, being configured as a synchronization master, wherein the transmitter transmits message frames having multiplexed data and direct data. (see Voth col. 3, lines 1-9)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability to be configured as a synchronization master. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 13, Voth discloses the time synchronization apparatus of claim 7, wherein the timing system is adjustable according to information received from the host processor. (see Voth col. 2, lines 51-54)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the timing system is adjustable. One

of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 14, Voth discloses the time synchronization apparatus of claim 1, being configured as a synchronization slave, wherein the receiver receives message frames at a fixed period, and wherein the timing system is adjusted according to the fixed period. (see Voth col. 4, lines 43-47)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability to be configured as a synchronization slave. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 18, Voth discloses the time synchronization apparatus of claim 16, wherein the timing system is adjusted according to the LCM indicator. (see Voth col. 4, lines 47-44)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the timing system is adjusted. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network

configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 19, Voth discloses the time synchronization apparatus of claim 16, wherein the receiver interrupts the host processor according to the LCM indicator. (see Voth col. 4, lines 43-47)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the receiver interrupts the host processor. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 20, Voth discloses the time synchronization apparatus of claim 14, being configured to operate as a synchronization master, wherein the transmitter periodically transmits message frames at a fixed period. (see Voth col. 4, lines 43-47)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability to be configured to operate as a synchronization master. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 21, Voth discloses the time synchronization apparatus of claim 20, wherein the message frames received and transmitted by the receiver and transmitter, respectively, comprise multiplexed data and direct data. (see Voth col. 5, lines 18-25)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the message frames received and transmitted comprise multiplexed data and direct data. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claims 22, 43, Voth discloses the time synchronization apparatus of claim 21, 39, wherein the data field comprises 6 32-bit words, and wherein the amount of multiplexed data and the amount of direct data in each message frame is configurable. (see Voth col. 5, lines 50-59; col. 6, lines 10-14: *"Different implementations of the present invention may use difference sizes for an, or all, of these components."*, where reference states that different sizes and values (i.e. amounts of data: 32 bit words) can be used for the data contained within message frames and therefore is configured by implementation.)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the data field comprises 6 32-bit words. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of

network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 23, Voth discloses the time synchronization apparatus of claim 22, wherein each message frame comprises a direct data portion and a multiplexed data portion, wherein the direct data comprises the direct data portion of a single frame, and wherein the multiplexed data comprises the multiplexed data portions of a plurality of frames. (see Voth col. 5, lines 18-25)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where each message frame comprises a direct data portion and a multiplexed data portion. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 24, Voth discloses the time synchronization apparatus of claim 23, wherein the multiplexed data portion comprises configuration information indicative of the amount of multiplexed data and the amount of direct data in each message frame. (see Voth col. 5, lines 26-29; col. 5, lines 50-59)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the multiplexed data portion comprises configuration information. One of ordinary skill in the art would have been motivated to

employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claims 25, 26, Voth discloses the time synchronization apparatus of claim 24, wherein the receiver presents direct data or multiplexed data from received message frames to the host processor at the fixed or a multiple of the fixed period. (see Voth col. 4, line 67 - col. 5, line 5)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the receiver presents direct data or multiplexed data from received message frames to the host processor. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 27, Voth discloses the time synchronization apparatus of claim 14, comprising a multiplier receiving an operand from the receiver, a multiplication value on the host processor, and providing a multiplication result value to at least one of the host processor and the transmitter, wherein the multiplication result value is the product of the multiplication value and the operand. (see Voth col. 5, lines 18-20)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability comprising a multiplier receiving an operand

from the receiver. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claims 28, 32, Voth discloses the time synchronization apparatus of claim 27, 30, wherein the direct data received in the message frame comprises the operand. (see Voth col. 5, lines 18-25)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the direct data received in the message frame comprises the operand. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 31, Voth discloses the time synchronization apparatus of claim 30, wherein at least a portion of the direct data in the message frames transmitted by the transmitter is provided to the transmitter by the receiver, wherein the direct data from a received message frame is passed through to the transmitter. (see Voth col. 6, lines 31-37)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where at least a portion of the direct data in

the message frames is provided to the transmitter by the receiver. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claims 33, 34, Voth discloses the time synchronization apparatus of claim 30, wherein at least a portion of the direct data and multiplexed data in the message frames transmitted by the transmitter is provided to the transmitter by the host processor. (see Voth col. 5, lines 20-25)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where at least a portion of the direct data and multiplexed data in the message frames is provided to the transmitter by the host processor. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 38, Yamanaka discloses a synchronization module in a control chassis for synchronizing operation of a first controller in the control chassis with that of a second controller outside the control chassis, comprising:

- a host processor in communication with the first controller via a backplane bus in the control chassis; (see Figure 3A; Figure 3B; col. 1, lines 15-22; col. 2, lines 29-

37)

- a synchronization circuit operatively associated with the host processor, the transmitter, the receiver, and the timing system, and configurable by the host processor to operate the module as one of a synchronization master and a synchronization slave. (see Figure 3A; col. 5, lines 5-9: configurable to operate as a master; Figure 3B; col. 5, lines 12-18: configurable to operate as a slave)

Yamanaka discloses a low bandwidth modem circuit for network connections in the network receipt of synchronization information and data. This type of network affords limited communications bandwidth and a limited number of possible network configurations and topologies.

However, Voth discloses wherein:

- a transmitter adapted to transmit synchronization information and data to a network in the control system; (see Voth col. 2, lines 57-60)
- a receiver adapted to receive synchronization information and data from the network; (see Voth col. 2, lines 60-61)
- a timing system with a clock and maintaining an indication of time according to information received from one of the network and the host processor; (see Voth col. 2, lines 51-54)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability to network communications in a variety of configurations. One of ordinary skill in the art would have been

motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 39, Yamanaka discloses a synchronization circuit for synchronizing operation of a first controller with that of a second controller in a control system, comprising:

- a processor interface for interfacing the synchronization circuit with a host processor; (see Yamanaka col. 1, lines 15-22; col. 2, lines 29-37)
- a timing system with a clock and maintaining an indication of time according to information received from one of the network and the host processor, wherein the synchronization circuit is configurable by the host processor to operate as one of a synchronization master and a synchronization slave. (see Yamanaka Figure 3A; col. 5, lines 5-9: configurable to operate as a master; Figure 3B; col. 5, lines 12-18: configurable to operate as a slave)

Yamanaka discloses a low bandwidth modem circuit for network connections in the network receipt of synchronization information and data. This type of network affords limited communications bandwidth and a limited number of possible network configurations and topologies.

However, Voth discloses wherein:

- a transmitter component adapted to transmit synchronization information and data

to a network in the control system; (see Voth col. 2, lines 57-60)

- a receiver component adapted to receive synchronization information and data from the network; (see Voth col. 2, lines 60-61) and

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability to network communications in a variety of configurations. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claims 40, 41, Voth discloses the system of claim 39, wherein the transmitter component periodically transmits message frames comprising direct data, and wherein the direct data is obtained from at least one of the receiver, the host processor, and the multiplier. (see Voth col. 5, lines 18-25)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the transmitter component periodically transmits message frames. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 42, Voth discloses the system of claim 39, wherein the transmitter

component periodically transmits message frames comprising multiplexed data, and wherein the multiplexed data is obtained from the host processor. (see Voth col. 4, lines 43-47)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the transmitter component periodically transmits message frames comprising multiplexed data. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 44, Voth discloses the system of claim 39, wherein the receiver component periodically receives message frames comprising direct data, multiplexed data, and status information from the network, and wherein the synchronization circuit provides at least one of received direct data, received multiplexed date and received status information from the receiver component to the host processor. (see Voth col. 6, lines 31-37)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the receiver component periodically receives message frames comprising direct data, multiplexed data, and status information. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col.

2, lines 39-43)

Regarding Claim 45, Voth discloses the system of claim 44, further comprising a multiplier operating on the received direct data, and wherein the synchronization circuit provides a multiplier result value from the multiplier to the host processor. (see Voth col. 5, lines 18-20)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability comprising a multiplier operating on the received direct data. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 46, Voth discloses the system of claim 45, wherein the synchronization circuit provides a multiplication value to the multiplier from the host processor. (see Voth col. 5, lines 18-20)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the synchronization circuit provides a multiplication value to the multiplier. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 48, Voth discloses the system of claim 39, wherein the transmitter component periodically transmits message frames comprising direct data, multiplexed data, and configuration information, and wherein the synchronization circuit provides at least one of the direct data, multiplexed data, and configuration information to the transmitter component from the host processor. (see Voth col. 5, lines 18-25)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the transmitter component periodically transmits message frames comprising direct data, multiplexed data, and configuration information. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 49, Voth discloses the system of claim 39, wherein the transmitter component periodically transmits message frames having synchronization information, wherein the synchronization information is obtained from the timing system, and wherein the timing system is adjusted according to at least one of synchronization information received from the network and synchronization information from the host processor. (see Voth col. 4, lines 43-47; col. 2, lines 51-54)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the transmitter component periodically

transmits message frames having synchronization information. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 50, Voth discloses the system of claim 39, wherein the synchronization circuit interrupts the host processor according to receipt of an LCM indicator by the receiver. (see Voth col. 4, lines 43-47)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the synchronization circuit interrupts the host processor. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 51, Voth discloses the system of claim 39, wherein the synchronization circuit interrupts the host processor periodically for presentation of at least one of direct data and multiplexed data from the receiver to the host processor. (see Voth col. 4, lines 43-47)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the synchronization circuit interrupts the host processor periodically. One of ordinary skill in the art would have been

motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 52, Voth discloses a synchronization system for synchronizing a first controller with a second controller in a control system, comprising:

- means for interfacing the synchronization circuit with a host processor; (see Figure 3A; Figure 3B; col. 1, lines 15-22; col. 2, lines 29-37)
- means for maintaining an indication of time according to information received from one of the network and the host processor, wherein the synchronization circuit is configurable by the host processor to operate as one of a synchronization master and a synchronization slave. (see Figure 3A; col. 5, lines 5-9: configurable to operate as a master; Figure 3B; col. 5, lines 12-18: configurable to operate as a slave)

Yamanaka discloses a low bandwidth modem circuit for network connections in the network receipt of synchronization information and data. This type of network affords limited communications bandwidth and a limited number of possible network configurations and topologies.

However, Voth discloses wherein:

- means for transmitting synchronization information and data to a network in the control system; (see Voth col. 2, lines 57-60)

- means for receiving synchronization information and data from the network; (see Voth col. 2, lines 60-61)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability to network communications in a variety of configurations. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claims 53, Voth discloses the time synchronization apparatus of claim 1, the synchronization apparatus exists in a different synchronization time zone from that of the host processor. (see Voth col. 4, lines 17-19: distributed internetworking environment such as the Internet operates across time zones)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the synchronization apparatus exists in a different synchronization time zone. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

5. **Claims 8, 9, 10, 11, 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yamanaka-Voth** and further in view of **Ramussen et al.** (US Patent No. **6,449,732**: Method and apparatus for processing control using a multiple redundant

processor control system).

Regarding Claim 8, Voth discloses a header with flag bytes, a control byte and a data field and a bitmask used in error detection for data within the message frames. Voth does not disclose specifically the CRC technique in error detection procedures. However, Rasmussen discloses the time synchronization apparatus of claim 7, wherein the same comprises three flag bytes, a control byte, a data field comprising the multiplexed data and the direct data, and two CRC bytes. (see Rasmussen col. 14, lines 1-4: *"Calculates and check the received CRCs…"* ; col. 14, lines 16-19: *"Calculates and send the transmit CRCs…"*)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability for a header with flag bytes, a control byte and a data field and a bitmask used in error detection for data within the message frames, and to modify Yamanaka-Voth with the error detection capabilities as taught by Rasmussen. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies (see Voth col. 2, lines 27-30; col. 2, lines 39-43), and to employ the invention of Rasmussen in order to enhance the processing of time synchronization information with an extension in error detection capabilities (see Rasmussen col. 5, lines 24-27: *"…hardware loop-back fault detection, CRC checking…."*).

Regarding Claims 9, 12, Voth discloses the time synchronization apparatus of claim 8, wherein the data field comprises 6 32-bit words, and wherein the amount of multiplexed data and the amount of direct data in each message frame is configurable. (see Voth col. 5, lines 50-59; col. 6, lines 10-14: *"Different implementations of the present invention may use difference sizes for an, or all, of these components."*, where reference states that different sizes and values (i.e. amounts of data: 32 bit words) can be used for the data contained within message frames and therefore is configured by implementation.)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the data field comprises 6 32-bit words. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 10, Voth discloses the time synchronization apparatus of claim 9, wherein each message frame comprises a direct data portion and a multiplexed data portion, wherein the direct data comprises the direct data portion of a single frame, and wherein the multiplexed data comprises the multiplexed data portions of a plurality of frames. (see Voth col. 5, lines 18-25)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where each message frame comprises a

direct data portion and a multiplexed data portion. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 11, Voth discloses the time synchronization apparatus of claim 10, wherein the multiplexed data portion comprises configuration information indicative of the amount of multiplexed data and the amount of direct data in each message frame. (see Voth col. 5, lines 26-32; col. 5, lines 48-59)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the multiplexed data portion comprises configuration information. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

6. **Claims 29, 35, 36, 37, 47** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yamanaka-Voth** and further in view of **Kuribayashi et al.** (US Patent No. **6,775,246**: Method of determining master and slaves by communication capability of network nodes).

Voth discloses a time synchronization apparatus with designated master and slave nodes and a timing system with a periodic and continuously updating feature.

(see Voth col. 35, lines 45: *"… a distributed system that maintains the synchronization between time clocks …, one of the nodes…assumes a master role. The remaining nodes 102 then function as slaves …To synchronize time clocks 212, master node 102a and slave nodes 102b-d use a repeating update cycle …."*)

Regarding Claims 29, 47, Voth does not disclose an apparatus to process status information from an upstream device. However, Kuribayashi discloses the time synchronization apparatus of claim 14, 44, wherein the message frame comprises a status component indicative of the status of an upstream device and error counter, wherein the receiver provides the status component to the host processor. (see Kuribayashi col. 2, lines 9-19; col. 8, lines 37-42)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yamanaka-Voth with an apparatus to process status information from an upstream device as taught by Kuribayashi. One of ordinary skill in the art would be motivated to employ the invention of Kuribayashi in order to extend the processing of time synchronization information to control the operation of additional devices. (see Kuribayashi col. 1, lines 53-57: *"…provide a novel communication control apparatus, which permits the proper and simple setting of transmission/reception nodes…synchronization information in a high-speed network."*)

Regarding Claim 35, Voth does not disclose a procedure to process a status signal from an upstream device in a daisy-chain. However, Kuribayashi discloses the time

synchronization apparatus of claim 1, being configured as an intermediate node in a daisy-chain topology, the receiver receiving synchronization information from an upstream device in the daisy-chain, and the transmitter transmitting the synchronization information to at least one downstream device in the daisy-chain. (see Kuribayashi col. 2, lines 9-19; col. 8, lines 37-42)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yamanaka-Voth in order for an apparatus to process status information from an upstream device as taught by Kuribayashi. One of ordinary skill in the art would be motivated to employ the invention of Kuribayashi in order to extend the processing of time synchronization information controlling the operation of networked devices. (see Kuribayashi col. 1, lines 53-57: *"...provide a novel communication control apparatus, which permits the proper and simple setting of transmission/reception nodes ...synchronization information in a high-speed network."*)

Regarding Claim 36, Voth discloses the time synchronization apparatus of claim 35, wherein the receiver receives message frames at a fixed period, and wherein the transmitter transmits message frames at the fixed period comprising direct data and multiplexed data. (see Voth col. 4, lines 47-54)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where the receiver receives message frames at a fixed period. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over

a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

Regarding Claim 37, Voth discloses the time synchronization apparatus of claim 36, wherein at least a portion of the direct data in the message frames transmitted by the transmitter is provided to the transmitter by the receiver, wherein the direct data from a received message frame is passed through to the transmitter. (see Voth col. 4, lines 47-54)

It would have been obvious to one of ordinary skill in the art to modify Yamanaka as taught by Voth to enable the capability where at least a portion of the direct data in the message frames transmitted by the transmitter is provided to the transmitter and the direct data from a received message frame is passed through to the transmitter. One of ordinary skill in the art would have been motivated to employ the teachings of Voth in order to enable the capability to network communications over a wide range of network configurations and topologies. (see Voth col. 2, lines 27-30; col. 2, lines 39-43)

(10) Response to Argument

A. Whether claims **1, 3-7, 13-28, 30-34, 38-46 and 48-53** are unpatentable under 35 U.S.C. §103(a) over Yamanaka, et al. (US 4,807,259) in view of Voth (US 6,199,169).

B. Whether claims **8-12** are unpatentable under 35 U.S.C. § 103(a) over Yamanaka, et al. (US 4,807,259) in view of Voth (US 6,199,169) in further view of Ramussen, et al.

(US 6,449,732).

C. Whether claims **29, 35-37, and 47** are unpatentable under 35 U.S.C. § 103(a) over Yamanaka, et al. (US 4,807,259) in view of Voth (US 6,199,169) in further view of Kuribayashi, et al. (US 6,775,246).

A. Whether claims **1, 3-7, 13-28, 30-34, 38-46 and 48-53** are unpatentable under 35 U.S.C. §103(a) over Yamanaka, et al. (US 4,807,259) in view of Voth (US 6,199,169). Applicant argues in substance that:

A.1: The referenced prior art discloses, "an inoperative combination". (Appeal Brief Page 6)

Applicant mentions that Voth (see Appeal Brief Page 8) was rejected as materially deficient to disclose the synchronization apparatus of the subject claims. The BPA stated that, "we did not review claims 2-52 to the extent necessary to determine whether these claims are patentable over the Voth patent or other cited references". The BPA decision states that the host interface for the time synchronization apparatus as claimed in claim 1 was not adequately disclosed within the Examiner's Answer or the latest Office Action. In response, Yamanaka discloses a host interface between a host and a clock apparatus used for time synchronization. (Yamanaka Figure 3A; Figure 3B; col. 1, lines 15-22; col. 2, lines 29-37; Figure 3A; col. 5, lines 5-9: configured to operate as a master; Figure 3B; col. 5, lines 12-18: configured to operate as a slave)

Applicant has stated that the examiner mentioned technological advances as

allowing Voth to operate successfully. (Appeal Brief Page 10) The Examiner is not aware of any indication that technological advances are required for Voth to operate. The Examiner stated that the operation of Voth is "possible" utilizing a high speed network. The features are disclosed by the referenced prior art and their successful operation are "possible" and therefore successfully disclosed.

Applicant has indicated a calculation using an alleged current processor speeds and a parameter of 1 billion ticks per seconds. (Appeal Brief Page 10) The assumptions used by the applicant use current statistics (processor speeds) and not year 2000 statistics. The application was initiated in the year 2000. The processor speed or clock speed indicates how many instructions the processor can execute in a designated time period. The "tick" applicant is trying to relate to is the quanta parameter indicated in Voth. (Voth col 8, ll 58-60: quanta value known as a tick) There is no indication this value in Voth is related to instruction processing. The processor execution time for an instruction can vary based on the complexity of the instruction (addition, exponentiation) This "tick" may be used in the determination of clock resolution in a UNIX type computer system. But, this "tick" has no relation to the clock speed or how many instructions a processor can execute within a designated time period. Based on these calculations applicant has indicated that the Voth method of synchronization would be incapable of functioning at inter-node distances greater that about 0.835 meters. (Appeal Brief Pages 10 and 12) It is unclear what applicant's calculations are trying to indicate since the calculations are using unrelated parameters. The resulting numbers have no significance to the referenced prior art.

The "trick" of Voth does not assume delay is zero. (Appeal Brief Page 9) The added feature of Voth assumes that the delay can be different for the send and receive transmissions. (Voth col 2, ll 10-13; col 2, 27-30) Applicant's cited sections merely indicate the ethernet simplification as the assumption of send and receive times are equal (there is no added congestion on the two transmissions (send and receive) of data). (Voth col 2, ll 44-47: synchronize system clocks; minimally affected by communications traffic)

Applicant has mentioned an ethernet simplification in network communications for Voth and this feature indicates that Voth distinguishes itself from Yamanaka. (Appeal Brief Page 9) Voth discloses there is a need for systems where the ethernet simplification does not apply and that the Voth invention has an additional feature used to provide a system where the ethernet simplification does not apply. (Voth col 2, ll 27-30: need for a network where ethernet simplification does not apply) The ethernet simplification is based on the network nodes having a single connection between endpoints of a communications link and the calculation of delay. Yamanaka does not disclose separate connections for the transmission of information between nodes therefore the standard single connection used for send/receive communication is implied. The Yamanaka system will still work within the Voth system environment. The Voth invention has additional features but these additional features do not remove the fact that Yamanaka and Voth are time synchronization systems. Both systems have master and slave designated nodes. Both systems pass information as

messages between master and slave nodes to provide time synchronization. How this feature indicated by applicant leads to the statement that Voth distinguishes itself from Yamanaka is unclear. From all indications the Voth and Yamanaka combination would successfully operate.

Applicant argues that a message will be rejected if the maximum round trip time is greater than half of a clock tick. (Appeal Brief Page 9) Voth states that a message (i.e. SYNC message) will be rejected if the time stamp difference (round trip time) value exceeds a predefined threshold. There is no mention of a 1/2 clock tick in the indicated citation. (Voth col 6, ll 50-53)

A.2: The referenced prior art does not discloses a fixed time period. (Appeal Brief Page 11)

The claim limitation indicates "about 50μs". (Appeal Brief Page 11, Line 20 and claim 4) The term "about" tends to make this a vague and indefinite value. The value could be just about any number value (50 or any value) used for a time interval. In addition, applicant states that Voth would perform an update an "excessive" number of times and waste processor power. This statement does not remove the fact that Voth discloses a fixed time period as an update cycle. Applicant has alleged that the parameter and its associated calculations are evidence that the Voth system is inoperative.

Applicant argues the LCM is not associated with the update cycle or periodic tasks

but, the specification states that the LCM (least common multiple) is a multiple (or could be 1) of the periodic update cycle. Applicant's specification states on page 13 at lines 20-26 that "...least common multiple (LCM) period ...can be set to the lowest integer multiple of periodic tasks..." (i.e. set to 1) Thus, the LCM is tied to the invention's periodic update cycle.

A.3: The referenced prior art does not disclose the time synchronization system being "configurable to operate as both a synchronization master and a synchronization slave". (Appeal Brief Page 7)

Yamanaka discloses the host interface between a host and a clock apparatus. Yamanaka clearly discloses the existence of master clocks and slave clocks. Yamanaka does not discourage the configurability of a host system as a slave or a master, therefore does not teach away from this feature within Voth. Voth discloses that one of the time synchronization nodes assumes a master role which is equivalent to one of the nodes being configured as a master. One network node is a master node and the other nodes are slave nodes. The claim limitation discloses the designation or configuration of a clock as a master and the designation or configuration of a clock as a slave. Yamanaka and Voth reject the master/slave configuration limitation.

The time synchronization system is operational on the UNIX system, which is operational by a host processor. The time synchronization system software (on one UNIX system) under the control of the host processor assumes or designates this time synchronization system as the master. This is equivalent to applicant's limitation that a

time synchronization system is configured as a master by the host (system).

Both Yamanaka and Voth disclose the existence of a master time synchronization apparatus and a slave time synchronization apparatus. (Yamanaka Figure 3A; Figure 3B; col. 1, lines 15-22; col. 2, lines 29-37; Figure 3A; col. 5, lines 5-9: configurable to operate as a master; Figure 3B; col. 5, lines 12-18: configurable to operate as a slave) And, Voth discloses that one node assumes master status (see Voth col. 4, lines 35-42: master node) and is configured to perform the master node time synchronization type functions. (see Voth col. 10, lines 44-45; col. 10, lines 53-55; col. 13, lines 61-62; col. 14, lines 9-10: configuration of master node)

A.4: The referenced prior art does not disclose operations within time zones. (Appeal Brief Page 12)

A time synchronization apparatus has as its basis a time parameter which is principally the current time value for a computer system within a particular time zone. Voth discloses a time synchronization apparatus operational within a distributed computer systems operational over the Internet (a global interconnected network with multiple time zones). Voth disclose ethernet type network (Voth col 2, l 11) as the operational environment for the time synchronization system, therefore Voth discloses systems operational across time zones. Two time synchronization systems at the border between two time zones (east and central time zones) can operation in different time zones and only be a few feet apart if each system is in a different time zone.

B. Whether claims **8-12** are unpatentable under 35 U.S.C. § 103(a) over Yamanaka, et al. (US 4,807,259) in view of Voth (US 6,199,169) in further view of Ramussen, et al. (US 6,449,732).

B.1: Applicant argues, "the dependent claims". (Appeal Brief Pages 12-13)

Arguments for dependent claims are based upon above arguments for independent claims 1. The successful responses to arguments for independent claims 1, also successfully respond to the current arguments against the dependent claims 8 - 12.

C. Whether claims **29, 35-37, and 47** are unpatentable under 35 U.S.C. § 103(a) over Yamanaka, et al. (US 4,807,259) in view of Voth (US 6,199,169) in further view of Kuribayashi, et al. (US 6,775,246).

C.1: The referenced prior art does not disclose a daisy-chain topology. (Appeal Brief Page 13)

The specification states that the communications network can be in a variety of configurations. (Specification Page 4, Lines 24-26: synchronization components can be configured in a variety of topologies, such as start, daisy-chain, loop configurations; as well as combinations thereof) In addition, the specification discloses that Ethernet can be a basis for the communications topology. (Specification Page 17, Lines 15-17) It is well known in the art that Ethernet provides for star and daisy-chain (or serial) topologies for the interconnected network nodes.

Voth discloses ethernet type communications used for interconnecting the network nodes or time synchronization systems. (Voth col. 2, l 11: ethernet type networks)

Voth discloses the usage of any number of different types of network and configurations (see Voth col. 4, lines 17-21), such as a star configuration or a daisy chain configuration. Voth and Kuribayashi discloses the capability to send and receive (control and non-control) information in a daisy-chain topology, the receiver receiving synchronization information from an upstream device in the daisy-chain, and the transmitter transmitting the synchronization information to at least one downstream device in the daisy-chain. (see Kuribayashi col. 2, lines 9-19; col. 8, lines 37-42) Ethernet can be implemented in a star configuration

Not only one skilled in the art knows the concept of data and non-data transfers between networked connected systems, but also, Voth discloses the same concept inherently as above (see Voth col. 2, lines 10-13). Although, Voth discloses the transmission of messages (i.e. data) between network connected systems in order to respond with a better explanation to remarks, the explicit disclosure of Kuribayashi prior art was introduced.

Voth discloses transmitting time synchronization information and non synchronization data over a network environment. As a further disclosure, Voth and Kuribayashi disclose the capability to transmitting time synchronization information and non time synchronization data over an interconnected network. (see Kuribayashi col. 8, lines 29-34; col. 9, lines 2-4: clock signals (i.e. time synchronization information) and

transmitting and receiving data (i.e. non time synchronization data))

Voth discloses that two systems or nodes are time synchronized. (see Voth col. 4, lines 17-27) A second UNIX type time synchronization system configured as above discloses the second controller (i.e. a separate system in its own chassis). Voth discloses a set of computer systems interconnected to provide a single computer system. (Voth col. 1, ll 21-24: computers interconnected to provide a single computer system)

The referenced prior art are analogous art. Voth discloses a time synchronization system. (Voth col. 2, lines 51-53: time synchronization system), the Rasmussen discloses a time synchronization system (see Rasmussen col. 4, lines 57-59; col. 12, lines 31-35), and Kuribayashi discloses a time synchronization system. Applicant's invention discloses a time synchronization apparatus. Therefore, the set of referenced prior art is analogous and legitimate prior art and utilized to discloses applicant's invention.

Conclusion

Voth discloses a time synchronization system utilizing UNIX type system. Voth is suitable for a collection of individual computers (known as nodes) that are interconnected to provide a single computing system. (Voth col. 1, ll 21-24: collection of computers to provide a single computer system) The dedicated processor utilized within the time synchronization system is loaded only with the required operating

system features. The communications network utilized is a very high speed capable network and the communications speeds in the communications network are within the invention's specification. Therefore, these features (i.e. high speed communications, operating system loaded only with required features) make the prior art disclosure of the invention possible and operable. (see Voth col. 4, lines 19-21: high speed network) Despite the applicant's alleged calculations and statements that distances between systems must be negligible, the claims limitations as disclosed by the referenced prior art is possible and operable.

The referenced prior art discloses time synchronization system(s). The referenced prior art discloses a set of time synchronization nodes. One of the nodes is designated as a master and the remaining nodes are designated as slaves. The master node maintains time synchronization between itself (the master node) and the slave nodes by the transmission of control messages such as SYNC messages between the interconnected network nodes.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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July 30, 2008

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